WHAT IS CLAIMED IS:

1. A synchronous semiconductor memory device taking in external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor device comprising:

a data output terminal;

read means for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command for successively transferring said data to said data output terminal; and

compression means for carrying out a prescribed operation on said data read by said read means from said plurality of memory cells in response to a test mode designating signal for compressing said data to one-bit data and outputting the same.

2. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of data output terminals;

a plurality of read means provided respectively for said plurality of data output terminals for simultaneously reading data from a predetermined plurality of memory

cells in response to a read mode command for successively transferring said data to corresponding data output terminals;

a plurality of compression means respectively provided to said plurality of read means for carrying out a prescribed operation on said data read by corresponding read means from said plurality of memory cells thereby compressing said data to one-bit data; and

output means for generating outputs of respective compression means to corresponding data output terminals.

3. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of data output terminals;

a plurality of read means provided respectively to said plurality of data output terminals for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command;

compression means for carrying out a prescribed operation on said data read by said plurality of read means from said memory cells for compressing said data to one-bit data; and

output means for generating an output of said

compression means to a particular one of said plurality of data output terminals.

4. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks having memory cell arrays and having means for activating and precharging corresponding said memory cells on bank by bank basis;

a data output terminal provided in common for said plurality of banks;

read means provided for said plurality of banks for simultaneously reading data from a predetermined plurality of memory cells from a corresponding memory cell array in response to a read mode command for successively transferring said data to said data output terminal;

a plurality of first compression means provided respectively for banks for carrying out a prescribed operation on said data read by corresponding read means from said plurality of memory cells for compressing said data to one-bit data; and

second compression means for carrying out another prescribed operation on outputs of said plurality of first compression means for compressing said outputs to one-bit

data and outputting the same to said data output terminal.

5. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks having memory cell arrays and having means for activating and precharging corresponding memory cells, on bank by bank basis;

a plurality of data output terminals shared by said plurality of banks;

a plurality of read means provided respectively to said plurality of data output terminals of each said bank for simultaneously reading data from a predetermined plurality of memory cells from a corresponding memory cell array in response to a read mode command for successively transferring said data to corresponding data output terminals;

a plurality of first compression means provided respectively for said banks for carrying out a first operation on said data read by each said plurality of read means from said memory cells for compressing said data to one-bit data; and

second compression means for carrying out a second operation on outputs of said plurality of first

compression means for compressing said outputs to one-bit data and outputting the same.

6. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor device comprising:

a data input terminal;

selection means for simultaneously selecting a predetermined plurality of memory cells for writing data successively supplied to said data input terminal; and

write means for simultaneously writing test data being supplied to said data input terminal within one clock cycle of said clock signal in said memory cells selected by said selection means in response to a test mode designating signal.

7. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor device comprising:

a plurality of data input terminals;

selection means for simultaneously selecting a group of a predetermined number of memory cells for each of said plurality of data input terminals for writing data

successively supplied to each of said plurality of data input terminals; and

write means for simultaneously writing test data supplied to each of said plurality of data input terminals in one clock cycle in corresponding groups of said predetermined number of memory cells selected by said selection means in response to a test mode designating signal.

8. A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor device comprising:

a plurality of data input terminals;

selection means for simultaneously selecting a prescribed number of memory cells for each of said plurality of data input terminals; and

write means for simultaneously writing test data supplied to a particular one of said plurality of data input terminals in one clock cycle of said clock signal in said prescribed number of memory cells selected by said selection means in response to a test mode designating signal.

9. A synchronous semiconductor memory device

incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks including memory cell arrays and having means for activating and precharging corresponding said memory cells on bank by bank basis; and

activation means for simultaneously activating said plurality of banks in response to a test mode designating signal.

10. A synchronous semiconductor memory device comprising:

a memory cell array having a plurality of memory cells;

read means for simultaneously reading data of a prescribed number of memory cells from said memory cell array;

a first wired circuit having a plurality of n-channel insulated gate type field effect transistors each having a gate receiving said data read by said read means from said prescribed number of memory cells, said plurality of n-channel insulated gate type field effect transistors being connected to a first signal line in parallel with each other;

a second wired circuit having a plurality of p-

channel insulated gate type field effect transistors each having a gate receiving said data read by said read means from said prescribed number of memory cells, said p-channel insulated gate type field effect transistors connected to a second signal line in parallel with each other; and

logic means for carrying out a prescribed logic operation on outputs of said first and second wired circuits.

11. The device according to claim 10, wherein said first wired circuit further includes a p channel precharge transistor responsive to a precharge enable signal for precharge said first signal line to an operating power supply potential level, and a first latch means responsive to said precharge enable signal being inactive for latching a signal on said first signal line, and wherein said second wired circuit further includes an n channel precharge transistor responsive to said precharge enable signal for precharging said second signal line to a ground potential level, and a second latch means responsive to said precharge enable signal being inactive for latching a signal on said second signal line, and wherein said logic means includes gate means for determining that an output of said first latch means is coincident in logic with an output

of said second latch means to generate a pass signal indicating that all the prescribed number of memory cells are good.

12. A synchronous type semiconductor memory device operating in synchronization with a clock signal, comprising:

data output means for externally supplying applied data in synchronization with said clock signal;

a memory cell array having a plurality of memory cells;

selection means responsive to an address signal applied in synchronization with said clock signal for simultaneously selecting a predetermined number of memory cells in said memory cell array,

said predetermined number being a multiple of the number of data bits by which said data output means can externally supplied at a time;

read means responsive to a read mode designating signal applied in synchronization with said clock signal for simultaneously reading and storing data of said predetermined number of memory cells selected by said selection means; and

compression means responsive to a test mode designating signal designating a test mode of operation

for compressing the data of the predetermined number of cells stored in said read means to a one-bit data indicating whether or not a defective memory cell is included in said predetermined number of memory cells.

13. The device according to claim 12, wherein said data output means includes a data output terminal and an output buffer for buffering a received data signal and supplying the buffered received data signal to said data output terminal, and wherein said read means includes a plurality, equal to said predetermined number, of read registers provided respectively to said predetermined number of memory cells for storing data of corresponding memory cells.

14. The device according to claim 13, wherein said compression means supplies said one-bit data to said output buffer.

15. The device according to claim 13, wherein said compression means supplies said one-bit data to a pin terminal different from said data output terminal.

16. The device according to claim 12, wherein said compression means includes;

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data indicating the result of determination.

17. The device according to claim 16, wherein said precharge enable signal is made inactive when said read mode designating signal is applied and after said read means stores data of the predetermined number of memory cells.

18. The device according to claim 16, wherein said gate means includes a first gate responsive to said precharge enable signal for generating a signal turning off said plurality of first conductivity type field effect transistors, and a second gate responsive to said precharge enable signal for generating a signal turning off said plurality of second conductivity type field effect transistors.

19. The device according to claim 12, wherein said output means includes a plurality of data output terminals, and a plurality of output buffers provided respectively for said plurality of data output terminals, and wherein said read means includes a prescribed number of data registers for each of said plurality of output buffers, said prescribed number being equal to said predetermined number divided by the factor of said

multiple, and wherein said compression means includes a plurality of compressors provided to each of said prescribed number of read registers, each of said plurality of compressors compressing data stored in corresponding read registers of said prescribed number into a one-bit data.

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20. The device according to claim 19, wherein said plurality of compressors supplies respective one-bit data to corresponding output buffers for external supply through corresponding data output terminals.

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21. The device according to claim 19, wherein said compression means further includes a compressing unit for compressing outputs of said plurality of compressors into a final one-bit data to be externally supplied.

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22. The device according to claim 21, wherein said compressing unit includes gate means receiving said outputs of said plurality of compressors in parallel for performing a predetermined logical operation on the received outputs to generate said final one-bit data indicating logical matching of the received outputs.

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23. The device according to claim 22, wherein said

predetermined logical operation is a logical product operation.

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24. The device according to claim 21, wherein said compressing units includes a plurality of cascaded logic gates each provided for a predetermined set of compressors of said plurality of compressors and each for compressing outputs of a corresponding set of compressors to a one-bit data for transference to a subsequent logic gate.

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25. The device according to claim 21, wherein said compressing unit includes a plurality of first gates each provided for a predetermined set of compressors of said plurality of compressors and each for compressing outputs of a corresponding set of compressors into a one-bit data, and a second gate receiving outputs of said plurality of gates for compressing the received outputs to the final one-bit data.

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26. The device according to claim 21, further comprising switch means responsive to said test mode designating signal for transferring said final one-bit data to all said plurality of output buffers.

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27. The device according to claim 21, further

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comprising means responsive to said test mode designating signal for supplying said final one-bit data to a particular one of said plurality of output buffers.

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28. The device according to claim 21, further comprising a terminal provided separately from said plurality of data terminals, for receiving said final one-bit data from said compressing unit.

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29. The device according to claim 12, wherein said output means includes a plurality of data output terminals, and a plurality of output buffers provided respectively to said plurality of data output terminals, and wherein said read means includes a prescribed number of data registers for each of said plurality of output buffers, said prescribed number being equal to said predetermined number divided by the factor of said multiple, and wherein said compression means includes a compressor receiving outputs of all of said prescribed number of data registers in parallel, for converting the received outputs to the one-bit data.

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30. The device according to claim 29, wherein an output of said compressor is supplied to a particular one of said plurality of output buffers.

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31. The device according to claim 12, further comprising,

another memory cell array being identical in arrangement to said memory cell array,

another data output means identical in structure to said data output means,

another selection means identical in structure to said selection means,

another read means being identical in structure to said read means,

another compression means, identical in structure to said compression means, and

compressor responsive to said test mode designating signal for compressing outputs of said compression means and said another compression means into the one-bit data.

32. The device according to claim 30, wherein the set of means associated with said memory array and the set of additional means associated with said another memory array respectively form banks each accessed on a bank by bank basis, and wherein said synchronous type semiconductor memory device further comprises means responsive to said test mode designating signal for activating all said banks.

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~~33~~. The device according to claim ~~31~~, wherein said data output means and said another data output means share a data output terminal supplying an external data.

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~~34~~. The device according to claim ~~12~~, further comprising

data input means for receiving externally applied data to generate internal write data in synchronization with said clock signal, and data write means responsive to a write mode designating signal applied in synchronization with said clock signal for transferring data received from said data input means onto said predetermined number of memory cells selected by said selection means,

said data write means including means responsive to said test mode designating signal for simultaneously transferring the data received from input means to said predetermined number of memory cells.

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~~35~~. The device according to claim ~~34~~, wherein said data input means includes a plurality of data input terminals, and a plurality of input buffers provided respectively to said plurality of data input terminals, and said data write means includes a prescribed number of write registers provided per the input buffer, and means responsive to said test mode designating signal for

simultaneously activating all said prescribed number of write registers for each said input buffer.

36. The device according to claim 35, wherein said data write means includes means responsive to said test mode designating signal for transferring data received from a particular one of said plurality of input buffers to all said prescribed number of write registers for each said input buffer simultaneously.

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gate means responsive to a precharge enable signal being inactive for generating test data corresponding to the data stored in said read means,

first wired circuit including a plurality of first conductivity type field effect transistors provided respectively for said test data and having gates receiving corresponding test data and provided between a first signal line and a first fixed potential mode in parallel with other, and a second conductivity type field effect transistor responsive to said precharge enable signal for precharging said first signal line to a second fixed potential,

a second wired circuit including a plurality of second conductivity type field effect transistor provided respectively for said test data and having gates receiving corresponding test data and provided between a second signal line and the second fixed potential node in parallel with other, and a precharge transistor of the first conductivity type for precharging said second signal line to said first fixed potential in response to said precharge enable signal, and

generation means responsive to said precharge enable signal being inactive for determining whether signal potentials on said first and second signal lines are identical in logic to each other to generate said one-bit